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MESSAGE/INSTRUCTIONS

Re:

Interview Agenda for Interview on January 5, 2004

U.S. Patent Application No.: 10/717,622

Inventor: TAKAHASHI Our Ref. No.: 100353-00179

Dear Examiner Hoang,

Proposed Agenda

- 1. Discuss the differences between claim 5, 6 and 8 and Kawamura. Specifically, we propose to discuss the operation of the memory cell transistor in Kawamura and the use of the region SD1 as a drain during a read operation and the use of the region SD2 as a drain for the write verify operation.
- 2. If necessary discuss claim amendments that would distinguish Kawamura when filed with an RCE.

Please let me know if you have any questions.

My IIII

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Arent Fox erub

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